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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/824,978	04/02/2001	Kevin J. McGrath	5500-66000	1318

53806 7590 02/28/2006

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EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/824,978	MCGRATH ET AL.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-15,17-25 and 27-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _ is/are allowed.

6)☒ Claim(s) *1,4,11,14,21,24,31-44,48,49 and 52-55* is/are rejected.

7)☒ Claim(s) *2,3,5,7-10,12,13,15,17-20,22,23,25,27-30,45-47,50 and 51* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Note Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive (according to the decision on petition mailed 04/07/05), therefore, the finality of that action has been withdrawn.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 31-41, and 52-55 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 31-41, and 52-55 are not limited to tangible embodiments. In view of Applicant's disclosure, specification page 40 lines 24-28, the computer readable medium is not limited to tangible embodiments, instead being defined as including both tangible embodiments (e.g., disk, CD-ROM, and RAM) and

intangible embodiments (e.g., transmission media or signals). As such, the claim is not limited to statutory subject matter and is therefore non-statutory. It is suggested to clearly define the computer readable medium is limited to tangible embodiments such as disk, CD-ROM, and RAM.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 32, and 33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 32, line 2, it is not clear what is meant by "the plurality of instructions emulate the first instruction". How can the plurality of instructions be executed responsive to the first instruction (as indicated in claim 31, lines 1-2) and also emulate the first instruction ?

In claim 33, line 2, it is not clear what is meant by "in place of the first instruction". How can the plurality of instructions be executed responsive to the first instruction (as indicated in claim 31, lines 1-2) and also be executed in place of the first instruction ?

Applicant is required to review the claims and correct all language which does not comply with 35 U.S.C. § 112, second paragraph.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 11, 21, 31-33, and 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Kogge (U.S. Patent No. 5,475,856), herein referred to as Kogge'856.

Referring to claim 1, Kogge'856 discloses as claimed a processor comprising: a first register (IR 105 in processor 1,

see Fig. 3) configured to store a first target address (note instruction register IR inherently stores a fetched branch instruction containing a next instruction target address information especially in the horizontal type branch instructions); a second register (IR 105 in one of processors 2-N, see Fig. 3) configured to store a second target address (note as set forth above, instruction register IR inherently stores a fetched branch instruction containing a next instruction target address information); and an execution core (see Fig. 3, the processor comprising processors 1-N, see also col. 4, lines 38-40) coupled to the first register (IR 105 in processor 1, see Fig. 3) and the second register (IR 105 in one of processors 2-N, see Fig. 3), wherein the execution core is configured, responsive to a first instruction (see Col. 6, lines 21-22, and lines 38-40 when the processor 1 functions as a controller), to: (i) select the first target address from the first register (IR 105 in processor 1, see Fig. 3) as a next program counter address if a first operating mode (this is the situation when the SIMD mode is active, see Fig. 1a and see also col. 6, lines 34-37) is active in the processor, and (ii) select the second target address from the second register (IR 105 in one of processors 2-N, see Fig. 3) as the next program counter address if a second operating mode (this is the situation when the MIMD

mode is active, see also col. 8, lines 52-56 regarding a processor (one of the processors 2-N, see Figs. 1b and 3), proceeds to fetch instructions as an individual processor) is active in the processor; and wherein the execution core is configured to store a first address (the next instruction address following the first instruction will be saved in PC 103 see Fig. 3 after the first instruction has been executed in the situation when the branch is NOT TAKEN after resolving the condition and the decision for the branch has been made by the system) in the third register (PC 103, see Fig. 3) responsive to the first instruction, wherein the first address is an address of a second instruction following the first instruction. Note claim 31 recites the corresponding limitations as set forth in claim 1.

Referring to claim 11, Kogge'856 discloses as claimed an apparatus comprising: a first storage location (IR 105 in processor 1, see Fig. 3) corresponding to a first register, the first storage location storing a first target address (note instruction register IR inherently stores a fetched branch instruction containing a next instruction target address information); a second storage location (IR 105 in one of processors 2-N, see Fig. 3) corresponding to a second register, the second storage location storing a second target address

(note as set forth above, instruction register IR inherently stores a fetched instruction containing a next instruction target address information); a third storage location (PC 103, see Fig. 3); and a processor (see Fig. 3, the processor comprising processors 1-N, se also col. 4, lines 38-40) coupled to the first storage location and the second storage location, wherein the processor is configured, responsive to a first instruction (see Col. 6, lines 21-22, and lines 38-40 when the processor 1 functions as a controller), to: (i) select the first target address from the first storage location (IR 105 in processor 1, see Fig. 3) as a next program counter address if a first operating mode (this is the situation when the SIMD mode is active, see Fig. 1a and see also col. 6, lines 34-37) is active, and (ii) select the second target address from the second storage location (IR 105 in one of processors 2-N, see Fig. 3) as the next program counter address if a second operating mode (this is the situation when the MIMD mode is active, see also col. 8, lines 52-56 regarding a processor (one of the processors 2-N, see Figs. 1b and 3), proceeds to fetch instructions as an individual processor) is active, and wherein the processor in configured to store a first address (the next instruction address following the first instruction will be saved in PC 103 see Fig. 3 after the first instruction has been

executed in the situation when the branch is NOT TAKEN after resolving the condition and the decision for the branch has been made by the system) in the third storage location (PC 103, see Fig. 3) responsive to the first instruction wherein the first address is an address of a second instruction following the first instruction.

Referring to claim 21, Kogge'856 discloses as claimed a method comprising: selecting a first target address from a first register (IR 105 in processor 1, see Fig. 3) as a next program counter address responsive to a first operating mode (this is the situation when the SIMD mode is active, see Fig. 1a and see also col. 6, lines 34-37) during execution of a first instruction (see Col. 6, lines 21-22, and lines 38-40 when the processor 1 functions as a controller); selecting a second target address from a second register (IR 105 in one of processors 2-N, see Fig. 3) as the next program counter address responsive to a second operating mode (this is the situation when the MIMD mode is active, see also col. 8, lines 52-56 regarding a processor (one of the processors 2-N, see Figs. 1b and 3), proceeds to fetch instructions as an individual processor) during execution of the first instruction (since the first instruction in processor 1 determines either SIMD or MIMD mode, see also Col. 6, lines 21-22, and lines 38-40 when the

processor 1 functions as a controller and col. 13, lines 25-27); and storing a first address (the next instruction address following the first instruction will be saved in PC 103 see Fig. 3 after the first instruction has been executed in the situation when the branch is NOT TAKEN after resolving the condition and the decision for the branch has been made by the system) in a third register (PC 103, see Fig. 3) responsive to executing the first instruction wherein first address is an address of a second instruction following the first instruction.

As to claim 32, Kogge'856 also discloses, as best understood, the plurality of instructions (the micro-instructions after an instruction is decoded) emulate the first instruction (the instruction being decoded).

As to claim 33, Kogge'856 also discloses, as best understood, the plurality of instructions are executed in place of the first instruction (since both are executed inside the same Kogge'856's CPU).

As to claim 42, Kogge'856 also discloses: a computer system (see Fig. 3) comprising the processor (1-N processors) and a peripheral device (a monitor of the Kogge'856's system) configured to communicate (through internet line) between the computer system and another computer system (such as a server or another computer system in the internet).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 4, 14, 24, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kogge'856.

Kogge'856 discloses the claimed invention except for having the first operation mode including a default address size greater than 32 bits.

Actually, Kogge'856 discloses the claimed invention having the first operation mode including a default address size of 32 bits.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Kogge'856's system to comprise the first operation mode including a default address size greater than 32 bits in order to increase the address space for the Kogge'856's system for avoiding memory

latency. **Further, as shown in re Rose, 105 USPQ 237 (CCPA 1955), to make changes in size/range generally does not provide patentable weight to the claimed invention.**

10. Claims 43, 44, 48, 49, 52, and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kogge'856 in view of Tran et al. (U.S. Patent No. 6,014,734), herein referred to as Tran et al.'734.

Kogge'856 discloses the claimed invention in claims 43, 48, and 52 as set forth above in claim 1 except for explicitly showing having the operating mode selected from a plurality of operating modes responsive to the operand size of the first instruction.

Tran et al.'734 discloses the operating mode selected from a plurality of operating modes responsive to the operand size of the first instruction (see col. 19, lines 10-15, regarding having operand sizes of 8, 16, 9r 32-bits depending on the mode of processor or instruction).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Kogge'856's machine to comprise the operating mode selected from a plurality of operating modes responsive to the operand size of the first

instruction, as taught by Tran et al.'734, in order to be able to simultaneously handle different size of operands with different modes for using legacy software systems (see Col. 19, lines 19-25).

As to claims 44, 49, and 53, Tran et al.'734 also disclose the operand size being specified via a prefix of the first instruction (since a prefix is inside the instruction sets of the Tran et al.'734's system).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Kogge'856's machine to comprise the operand size being specified via a prefix of the first instruction, as taught by Tran et al.'734, in order to be able to facilitate selecting the operand size for simultaneously handle different size of operands with different modes for using legacy software systems (see Col. 19, lines 19-25).

Allowable Subject Matter

11. Claims 2, 3, 5, 7-10, 12, 13, 15, 17-20, 22, 23, 25, 27-30, 45-47, 50, and 51 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Amendment

12. Applicant's arguments mailed 10/29/04 have been considered but are moot in view of the new explanation and new ground(s) of rejection.

As set forth in the art rejections above, Kogge'856 and Tran et al.'734 teach the claimed invention

Contact Information

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Kim Huynh, can be reached on (571) 272-4147. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to **the TC central telephone number, 571-272-2100.**

14. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number: 571-273-8300.** This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER
February 21, 2006